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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,229	12/11/2003	Charles Frank Machala III	TI-36674	1860

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EXAMINER	
GOUDREAU, GEORGE A	
ART UNIT	**PAPER NUMBER**
1763	

DATE MAILED: 08/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/735,229	MACHALA, CHARLES FRANK	
	Examiner	Art Unit	
	George A. Goudreau	1763	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

George A Goudreau

GEORGE GOUDREAU
PRIMARY EXAMINER
8-05

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. This action will not be made final due to the new grounds of rejection.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner et. al. (5,863,824) further in view of Nandakumar et. al. (6,150,669).

Gardner et. al. disclose a process for fabricating a transistor comprised of the following steps:

-A gate dielectric layer (205) is formed onto the surface of a wafer (201).;

-A gate electrode (203) is formed onto the surface of the gate dielectric layer.;

-The gate dielectric layer, and the gate electrode are anisotropically etched.;

-The length of the gate electrode is measured using a SEM in the direction parallel to the channel and compared to targeted desired channel length.;

-A SiO2 layer (207) may optionally be deposited onto the surface of the wafer.;

-A spacer dielectric layer (209), which is comprised of Si3N4, is then conformably deposited onto the surface of the wafer. The thickness of the Si3N4 layer, which is deposited onto the surface of the wafer, is determined based upon ½ the difference between the measured gate length, and the targeted channel length.; and

-The spacer dielectric layer is then anisotropically etched to form the spacers on the sidewalls of the gate electrode.

This is discussed specifically in columns 2-5; and discussed in general in columns 1-6. This is shown in figures 1-3. Gardner et. al. fail, however, to specifically disclose the following aspects of applicant's claimed invention:

-the specific formation of the test structure in the scribe region of the wafer

Nandakumar et. al. teach that it is desirable to form test structures in the scribe line region of a wafer, which are used for the measurement of the gate line width. This is discussed specifically in the abstract; and discussed in general in columns 1-6. This is shown in figures 1-8.

It would have been desirable to form test structures in the scribe line region of the wafer in the process taught by Gardner et. al. as applied above based upon the following. Nandakumar et. al. teach that it is desirable to form test structures used in the measurement of gate line widths in the scribe line region of a wafer.

5. Applicant's arguments with respect to claims of record have been considered but are moot in view of the new ground(s) of rejection.

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

7. Any inquiry concerning this communication should be directed to examiner George A. Goudreau at telephone number (571)-272-1434.

George A. Goudreau
Primary Examiner
Art Unit 1763